

# PATENT ABSTRACTS OF JAPAN

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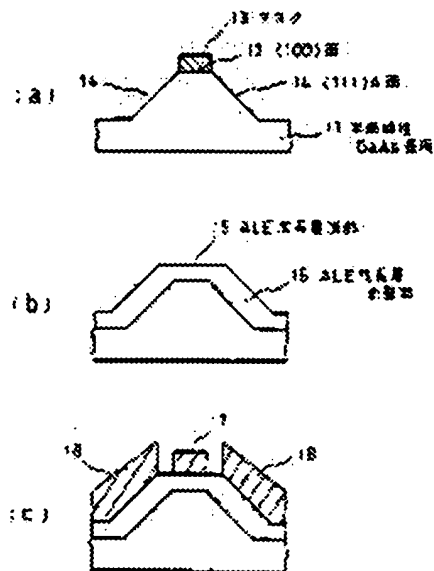
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## (54) III-V COMPOUND SEMICONDUCTOR FIELD-EFFECT TRANSISTOR AND MANUFACTURE THEREOF

### (57)Abstract:

**PURPOSE:** To form a FET of high quality having low source resistance of source, drain regions by providing the source, drain regions on the sidewall of plane 111A of a forward mesa structure formed on a semi-insulating substrate of plane 100 and a gate region on the surface of plane 100 of the top of the forward mesa structure.

**CONSTITUTION:** After the surface 12 of plane 100 to become a gate region of a semi-insulating GaAs substrate 11 is masked with an SiO<sub>2</sub> film 13 and the surface 14 of plane 111A to become source, drain regions is formed with etchant, the mask 13 is removed. Then, GaAs is ALE-grown on the substrate. An Se impurity is planely doped at each 10 layers of the GaAs. Eventually, a WSi heat resistant gate electrode 17 is formed on the top 15 of the ALE-grown layer, and contact electrodes 18 to become source, drain are formed on the wall 16 of the ALE-grown layer side by alloying AuGe alloy and an n-type layer. Thus, the contact resistivity of the source, drain regions with the electrodes is extremely reduced, and preferable FET characteristics are obtained.



## LEGAL STATUS

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